I. **INTRODUCTION**
   A. Programmable Logic Devices (PLDs) allow the user to define a function on single or multiple chips, rather than work around standard offerings from device manufacturers. Designs for these devices are developed with sophisticated computer programs taking advantage of the PC or workstation environment.

   B. This course is an introductory course in digital electronics in an electronics engineering technologist (EET) or computer engineering technologist (CET) program.

   C. Prerequisite: CETT-1425 and CETT-1429

II. **LEARNING OUTCOMES**

   Upon successful completion of this course, the student will be able to:

   A. Use Boolean Algebra to simplify circuits. *(F9)*
   B. Understand PLD structure and program devices using common software. *(F10)*
   C. Simulate circuit programs. *(C5, C8, F10)*
   D. Understand VHDL structures and language. *(F1, F10)*
   E. Create hierarchical designs to implement desired operations using VHDL and block diagrams. *(C8, F10, F12)*
   F. Create common sequential logic devices, counters, and shift registers using VHDL and block diagrams. *(C8, F11)*
   G. Work as a group member to integrate all of the above elements to design a unique operating circuit. *(C3, C4, C8, C9, C13, C14)*

III. **INSTRUCTIONAL MATERIALS**

   The instructional materials identified for this course are viewable through [www.ctcd.edu/books](http://www.ctcd.edu/books)
IV. COURSE REQUIREMENTS

A. Reading Assignments: Chapter text as assigned. The student may be quizzed at end of each chapter.

B. Class Performance: Students are required to be in class on time. Excessive tardiness (four) will result in a five point reduction to the final grade. It is the recommendation of this department that students exchange telephone numbers so that they may acquire missed lecture notes and assignments.

C. Class Participation: Students are expected to be interactive with the instructor during lecture. A question/response format will be used. Class participation is part of the Lab Experiment grade and is based on the amount of participation each student contributes to the lab’s results.

V. EXAMINATIONS

There will be two exams, a Mid-Term and a Final Exam, each covering the chapters completed in class. A general review will be given before each exam. Should a test be missed due to extenuating circumstances, you may contact the instructor for a make-up exam. Make-up exams may have more questions than the normally scheduled test. In addition to the two exams, other exams or quizzes may be given at the discretion of the instructor.

VI. SEMESTER GRADE COMPUTATION

<table>
<thead>
<tr>
<th>Component</th>
<th>Points</th>
<th>Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework/Quizzes</td>
<td>200</td>
<td>1000 – 900 = A</td>
</tr>
<tr>
<td>Exam One</td>
<td>200</td>
<td>899 - 800 = B</td>
</tr>
<tr>
<td>Exam Two</td>
<td>200</td>
<td>799 - 700 = C</td>
</tr>
<tr>
<td>Lab Projects</td>
<td>400</td>
<td>699 - 600 = D</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>1000</strong></td>
<td><strong>599 - 0 = F</strong></td>
</tr>
</tbody>
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Students who do not complete all projects successfully, with approval by the instructor, will receive an Incomplete for the course grade and will have three weeks into the next semester to finish the projects or their grade will become an F.
VII. ATTENDANCE

Students are required to attend all classes in which they have enrolled. Students are required to be in the classrooms on time and remain for the duration of the class. Any time a student has 10 hours absence, an administrative withdrawal will be submitted.

A. Four Classes of 2 ½ hours = 10 Hours
B. Late for Class = 1 Hour Absence: 10 Times = 10 Hours

VIII. NOTES AND ADDITIONAL INSTRUCTIONS FROM THE INSTRUCTOR

A. **Course Withdrawal**: It is the student’s responsibility to officially withdraw from a course if circumstances prevent attendance. Any student who desires to, or must, officially withdraw from a course after the first scheduled class meeting, must file a Central Texas College Application of Withdrawal (CTC Form 59). The withdrawal form must be signed by the student.

A student who officially withdraws will be awarded the grade of W provided the student’s attendance and academic performance are satisfactory at the time of official withdrawal. Students must file a withdrawal application with the College before they may be considered for withdrawal. A student may not withdraw from a class for which the instructor has previously issued the student a grade of F.

B. **Administrative Withdrawal**: An administrative withdrawal may be initiated when the student fails to meet College attendance requirements.

C. **Incomplete Grade**: The College catalog states an incomplete grade may be given in those cases where the student has completed the majority of the course work, but because of personal illness, death in the immediate family, or military orders, the student is unable to complete the requirements for a course. Prior approval from the instructor is required before the grade of “IP” for Incomplete is recorded. A student who merely fails to show for the final examination will receive a zero for the final and an F for the course.

D. **Cellular Phones and Beepers**: Cellular phones and beepers will be turned off while the student is in the classroom or laboratory.

E. **Americans with Disabilities Act (ADA)**: Disability Support Services provides services to students who have appropriate documentation of a disability. Students requiring accommodations for class are responsible for contacting the Office of Disability Support Services (DSS) located on the central campus. This service is available to all students, regardless of location. Explore the website at [www.ctcd.edu/disability-support](http://www.ctcd.edu/disability-support) for further information. Reasonable
accommodations will be given in accordance with the federal and state laws through the DSS office.

F. Instructor Discretion: The instructor reserves the right of final decision in course requirements.

G. Civility: Individuals are expected to be cognizant of what a constructive educational experience is and respectful of those participating in a learning environment. Failure to do so can result in disciplinary action up to and including expulsion.

IX. COURSE OUTLINE

A. Lesson One: Boolean Algebra and Combinational Logic

1. Lesson Objectives: Upon successful completion of this lesson, the student will be able to:

   a. Explain the relationship between the Boolean expression, logic diagram, and truth table of a logic gate network and be able to derive any one from either of the other two.
   b. Draw logic gate networks in such a way as to cancel out internal inversions automatically (bubble-to-bubble convention).
   c. Write the sum of products (SOP) or product of sums (POS) forms of a Boolean equation.
   d. Use rules of Boolean algebra to simplify the Boolean expressions derived from logic diagrams and truth tables.
   e. Apply the Karnaugh map method to reduce Boolean expressions and logic circuits to their simplest forms.
   f. Use a graphical technique based on DeMorgan equivalent gates to simplify logic diagrams.
   g. Redraw a logic diagram using all-NAND or all-NOR implementations.
   h. Draw logic circuits that account for the practical limitations of commercially available logic gates.
   i. Predict the response of a logic circuit to a time-varying input signal.
   j. Apply analysis tools to convert word problems to Boolean equations for the purposes of logic circuit design.

2. Learning Activities:

   a. Read Chapter 3 in the textbook. (F1)
   b. Complete assigned problems at end of the chapter. (F8, F9, F10)
   c. Complete projects as assigned. (C5, C8, F10, F12)
B. **Lesson Two: Introduction to PLDs and Quartus II**

1. **Lesson Objectives:** Upon successful completion of this lesson, the student will be able to:
   
a. Draw a diagram showing the basic hardware conventions for a sum-of-products-type programmable logic device.
   b. Describe the structure of a programmable array logic (PAL) AND matrix.
   c. Draw fuses on the logic diagram of a PAL to implement simple logic functions.
   d. Describe the structures of combinational PAL outputs, including those with programmable polarity.
   e. Determine the number and type of outputs from a PAL/GAL part number.
   f. Describe some advantages of programmable logic over fixed-function logic.
   g. Name some types of programmable logic devices (PLDs).
   h. Use Altera’s Quartus II PLD design software to enter simple combinational circuits using schematic capture.
   i. Create circuit symbols from schematic designs and use them in hierarchical designs for PLDs.
   j. Assign device and pin numbers to schematic designs and compile them for programming Altera MAX 7000S or FLEX 10K devices.
   k. Program Altera PLDs via a JTAG interface and a ByteBlaster Parallel Port Download Cable.

2. **Learning Activities:**
   
a. Read chapter 4 in the textbook. *(F1)*
   b. Complete assigned problems at end of the chapter. *(F8, F9, F10)*
   c. Complete projects as assigned. *(C5, C8, F10, F12)*

C. **Lesson Three: Introduction to VHDL**

1. **Lesson Objectives:** Upon successful completion of this lesson, the student will be able to:
   
a. State what VHDL stands for.
   b. State the functions of a VHDL entity declaration and architecture body.
   c. Write VHDL statements defining an entity and architecture, including ports, complete with mode and type.
d. Define and use BIT, STD_LOGIC, and INTERGER types.
e. Encode Boolean expressions in VHDL, using concurrent signal assignment statements.
f. Encode truth tables in VHDL, using selected signal assignment statements.
g. Use Quartus II software to enter, compile, and simulate a VHDL design.
h. Use Quartus II software to assign pins to a CPLD and program the CPLD.

2. **Learning Activities:**
   
a. Read Chapter 5 in the textbook. (F1)
b. Complete assigned problems at end of the chapter. (F8, F9, F10)
c. Complete projects as assigned. (C5, C8, F10, F12)

D. **Lesson Four: Combinational Logic Functions**

1. **Learning Objectives:** Upon successful completion of this lesson, the student will be able to:
   
a. Design binary decoders using logic gates.
b. Create decoder designs in Quartus II, using Block Diagram Files or VHDL.
c. Create Quartus II simulation files to verify the operation of combinational circuits.
d. Design BCD-to-seven-segment and hexadecimal-to-seven-segment decoders, including special features such as ripple blanking, using VHDL and Block Diagram Files in Quartus II.
e. Use Quartus II Block Diagram Files and VHDL to generate the design for a 3-bit binary and a BCD priority encoder.
f. Describe the circuit and operation of a simple multiplexer and program these functions in VHDL.
g. Draw logic circuits for multiplexer applications, such as single-channel data selection, multibit data selection, waveform generation, and time-division multiplexing (TDM).
h. Describe demultiplexer circuits and program them using VHDL.
i. Define the operation of a CMOS analog switch and its use in multiplexers and demultiplexers.
j. Define the operation of a magnitude comparator and program its function in VHDL.
k. Explain the use of parity as an error-checking system and draw simple parity-generation and checking circuits.

2. **Learning Activities:**
a. Read Chapter 6 in the textbook. (F1)
b. Complete assigned problems at end of the chapter. (F8, F9, F10)
c. Complete projects as assigned. (C5, C8, F10, F12)

E. **Lesson Five: Digital Arithmetic and Arithmetic Circuits**

1. **Lesson Objectives:** Upon successful completion of this lesson, the student will be able to:
   
a. Add or subtract two unsigned binary numbers.
b. Write a signed binary number in true-magnitude, 1’s complement, or 2’s complement form.
c. Add or subtract two signed binary numbers.
d. Explain the concept of overflow.
e. Calculate the maximum sum or difference of two signed binary numbers that will not result in an overflow.
f. Add or subtract two hexadecimal numbers.
g. Write decimal numbers in BCD codes, such as 8421 (Natural BCD) and Excess-3 code.
h. Construct a Gray code sequence.
i. Use the ASCII table to convert alphanumeric characters to hexadecimal or binary numbers and vice versa.
j. Derive the logic gate circuits for full and half adders, given their truth tables.
k. Demonstrate the use of full and half adder circuits in arithmetic and other applications.
l. Add and subtract \(n\)-bit binary numbers, using parallel binary adders and logic gates.
m. Explain the difference between ripple carry and parallel carry.
n. Design a circuit to detect sign-bit overflow in a parallel adder.
o. Draw circuits to perform BCD arithmetic and explain their operation.
p. Use VHDL to program CPLD devices to perform various arithmetic functions, such as parallel adders, overflow detectors, and 1’s complementers.

2. **Learning Activities:**
   
a. Read Chapter 7 of the textbook. (F1)
b. Complete assigned problems at end of chapter. (F8, F9, F10)
c. Complete projects as assigned. (C5, C8, F10, F12)

F. **Lesson Six: Introduction to Sequential Logic**
1. **Lesson Objectives:** Upon successful completion of this lesson, the student will be able to:

   a. Explain the difference between combinational and sequential circuits.
   b. Define the set and reset functions of an SR latch.
   c. Draw circuits, function tables, and timing diagrams of NAND and NOR latches.
   d. Explain the effect of each possible input combination to a NAND and a NOR latch, including set, reset, and no change functions, as well as the ambiguous or forbidden input condition.
   e. Design circuit applications that employ NAND and NOR latches.
   f. Describe the use of the ENABLE input of a gated SR or D latch as an enable/inhibit function and as a synchronizing function.
   g. Outline the problems involved with using a level-sensitive ENABLE input on a gated SR or D latch.
   h. Explain the concept of edge-triggering and why it is an improvement over level-sensitive enabling.
   i. Draw circuits, function tables, and timing diagrams of edge-triggered D, JK, and T flip-flops.
   j. Describe the toggle function of a JK flip-flop and a T flip-flop.
   k. Describe the operation of the asynchronous preset and clear functions of D, JK, and T flip-flops and be able to draw timing diagrams showing their functions.
   l. Use Quartus II to create simple circuits and simulations with D latches and D, JK, and T flip-flops.
   m. Create simple latch and flip-flop designs using VHDL.
   n. Describe the structure of registered PAL outputs.
   o. Determine the number and type of outputs from a PAL/GAL part number.
   p. Explain the structure of an output logic macrocell (OLMC).
   q. State differences between generic array logic (GAL) and standard PAL.
   r. Interpret the logic diagrams of GAL devices to determine the number of outputs and product terms and the type of control signals available in a device.
   s. Interpret block diagrams to determine the basic structure of an Altera MAX 7000S CPLD, including macrocell configuration, logic array blocks (LABs), control signals, and product term expanders.
   t. State the differences between PLDs based on sum-of-products (SOP) architecture versus look-up table (LUT) architecture.
   u. Interpret block diagrams to determine the basic structure of a logic element in an Altera FLEX 10K CPLD, including look-up tables, cascade chains, carry chains, and control signals.
v. Interpret block diagrams to determine how a logic element in a FLEX 10K device relates to the overall structure of the device.
w. Interpret block diagrams to determine how logic array blocks and embedded array blocks relate to the overall structure of a FLEX 10K CPLD.

2. **Learning Activities:**
   
a. Read Chapter 8 in the textbook. *(F1)*
b. Complete assigned problems at end of chapter. *(F8, F9, F10)*
c. Complete projects as assigned. *(C5, C8, F10, F12)*

G. **Lesson Seven: Counters and Shift Registers**

1. **Lesson Objectives:** Upon successful completion of this lesson, the student will be able to:
   
a. Draw the count sequence table, state diagram, and timing diagram of a counter.
b. Determine the recycle point of a counter’s sequence.
c. Calculate the frequencies of each counter output, given the input clock frequency.
d. Draw a circuit for any full-sequence synchronous counter.
e. Determine the count sequence, state diagram, timing diagram, and modulus of any synchronous counter.
f. Complete the state diagram of a synchronous counter to account for unused states.
g. Design the circuit of a truncated-sequence synchronous counter, using flip-flops and logic gates.
h. Use Quartus II to create a Block Diagram File for any synchronous counter circuit.
i. Use behavioral descriptions in VHDL to design synchronous counters of any modulus.
j. Use a parameterized counter from the Library of Parameterized Modules in a Block Diagram File and a VHDL file.
k. Use the Quartus II simulation tool to verify the operation of synchronous counters.
l. Implement various counter control functions, such as parallel load, clear, count enable, and count direction, both in Block Diagram Files and in VHDL.
m. Design a circuit to decode the output of the counter, both in a Quartus II Block Diagram File and in VHDL.
n. Draw a logic circuit of a serial shift register and determine its contents over time given any input data.
o. Draw a timing diagram showing the operation of a serial shift register.
q. Draw a timing diagram showing the operation of a parallel-load shift register.
r. Draw the general logic circuit of a bidirectional shift register and explain the concepts of right-shift and left-shift.
s. Use timing diagrams to explain the operation of a bidirectional shift register.
t. Describe the operation of a universal shift register.
u. Design shift registers, ring counters, and Johnson counters with the Quartus II Block Editor or VHDL.
v. Verify the operation of shift registers, ring counters, and Johnson counters using the Quartus II simulation tool.
w. Design a decoder for a Johnson counter.
x. Use a ring counter or a Johnson counter as an even sequencer.
y. Compare binary, ring, and Johnson counters in terms of the modulus and the required decoding for each circuit.

2. Learning Activities:

a. Read Chapter 9 of the textbook. (F1)
b. Complete assigned problems at end of the chapter. (F8, F9, F10)
c. Complete projects as assigned. (C5, C8, F10, F12)

H. Lesson Eight: Concept Integration and Design Project

1. Lesson Objectives: Upon successful completion of this lesson, the student will be able to:
a. Working as a group leader or team member, design a circuit to accomplish tasks as assigned by instructor
b. Draw the circuit’s schematic and timing charts.
c. Demonstrate the circuits operation and explain design elements to the class.

2. Learning Activities:

Same as objectives. (C3, C4, C8, C9, C13, C14)