I. INTRODUCTION

A. Since the introduction of the digital computer, the use of digital circuits has become extensive in all areas of electronics from the most sophisticated communication networks to the radio and television industry. This wide acceptance is due to their accuracy, dependability, and simplicity.

B. This course will cover the fundamentals of basic gate and gating networks in digital electronics as well as the reduction of gating networks through the use of Boolean algebra and Karnaugh Maps. Flip-flops and their use as registers, counters and control circuits will be studied. Numbering systems, adders, and other arithmetic circuits are also discussed.

C. Classes will be lecture and laboratory combination where the student will be studying basic principles of digital circuits and then applying these principles in practice using proto-boards and integrated circuits.

D. It is important that the student obtain a firm foundation in basic digital circuits as it is not only a required course in the Electronics curriculum, but it is also a fundamental course on which all advanced electronics build. There is no prerequisite for this course.

II. LEARNING OUTCOMES

Upon successful completion of this course, Digital Fundamentals, the student will be able to:

A. Explain the gray code, binary octal, hex codes, and how they relate to each other (F3, F4, F5, F11, C5, C8)

B. Differentiate between the different logic gates and explain how each gate functions and how it differs from other gates in that operation. (C6, F1, F5)

C. Construct gating networks and explain their simplification through the use of DeMorgan’s theorem, Boolean laws and identities. (F9, F10, F11, F12)

D. Solve problems in Boolean algebra and explain its application to digital circuits. (F9, F11, F12)
E. Differentiate between the types of Flip Flops and their operation. (C5, C6, C8, F1, F5, F8, F11)

F. Explain IC specifications, encoding, decoding, and displays. (F5, F11)

G. Identify the many different types of counters and how to construct them. (C5, C6, C8, F1, F5, F8, F11)

H. Solve binary arithmetic and explain how it is used in conjunction with half and full adders. (F3, F4, F6)

III. INSTRUCTIONAL MATERIALS

A. The instructional materials identified for this course are viewable through www.ctcd.edu/books

IV. COURSE REQUIREMENTS

A. The student must pass all quizzes with a 75 or higher. These quizzes must be completed no later than two weeks after they become available.

B. If a student experiences any difficulty, he/she should ask the instructor for assistance. It should be understood that the student is to have read the material and reviewed the associated PowerPoint slides first.

C. Homework will be turned in on time. Late or incomplete work will not be accepted.

D. Some experiments performed must be viewed by the instructor. A photo or video of the working circuit is acceptable for students in the Distance Learning class.

V. EXAMINATIONS

A. There will be a quiz on each of the six units covered. Each quiz earns a maximum of 75 points; all six quizzes are worth 450 points. There will be a final exam on all of the material studied.

B. The Final Examination will be Comprehensive. Failure to PASS this TEST will result in a maximum grade of “D” for the ENTIRE COURSE.
<table>
<thead>
<tr>
<th>Unit</th>
<th>Chapter</th>
<th>Topics</th>
<th>Test Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ch 1</td>
<td>Introduction</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Ch 2</td>
<td>Numbering Systems</td>
<td></td>
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<tr>
<td>3</td>
<td>Ch 3</td>
<td>Gates</td>
<td></td>
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<tr>
<td>4</td>
<td>Ch 4</td>
<td>Boolean Karnaugh Simplification</td>
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<tr>
<td>5</td>
<td>Ch 8 and 4</td>
<td>Integrated Circuit Logic Families Troubleshooting Digital Circuits</td>
<td></td>
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<tr>
<td>6</td>
<td>Ch 5</td>
<td>Latches/Flip-Flops</td>
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<tr>
<td>7</td>
<td>Ch 7</td>
<td>Counters</td>
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<tr>
<td>8</td>
<td>Ch 6</td>
<td>Arithmetic Circuits</td>
<td></td>
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</tbody>
</table>

**Final Exam**

### VI. SEMESTER GRADE COMPUTATION

<table>
<thead>
<tr>
<th>Activity</th>
<th>Points</th>
<th>Grade Range</th>
<th>Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit Quizzes</td>
<td>300</td>
<td>1000 – 900</td>
<td>A</td>
</tr>
<tr>
<td>Lab Work</td>
<td>400</td>
<td>899 – 800</td>
<td>B</td>
</tr>
<tr>
<td>Companion Site Quizzes</td>
<td>150</td>
<td>799 – 700</td>
<td>C</td>
</tr>
<tr>
<td>Homework</td>
<td>150</td>
<td>699 – 600</td>
<td>D</td>
</tr>
<tr>
<td>Final Exam</td>
<td>P/F</td>
<td>599 – 0</td>
<td>F</td>
</tr>
</tbody>
</table>

Total: 1000 points

Students who do not complete all projects successfully and receives an Incomplete for the course grade will have three weeks into the next semester to finish the projects. Failure to finish lab projects will result in a grade no higher than a D.

### VII. ATTENDANCE

Students are required to attend all classes in which they have enrolled. Students are required to be in the classrooms on time and remain for the duration of the class. Any time a student has 10 hours absence, an administrative withdrawal will be submitted.

A. Four Classes of 21/2 hours = 10 Hours
B. Late for Class = 1 Hour Absence: 10 Times = 10 Hours

### VIII. NOTES AND ADDITIONAL INSTRUCTIONS FROM COURSE INSTRUCTOR

A. Course Withdrawal: It is the student’s responsibility to officially withdraw from a course if circumstances prevent attendance. Any student who desires to, or must, officially withdraw from a course after the first scheduled class meeting must
file a Central Texas College Application of Withdrawal (CTC Form 59). The withdrawal form must be signed by the student.

CTC Form 59 will be accepted at any time prior to Friday of the 12th week of class during the 16-week fall and spring semesters. The deadline for sessions of the other lengths is:

<table>
<thead>
<tr>
<th>Session Length</th>
<th>Deadline</th>
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<tbody>
<tr>
<td>10-week session</td>
<td>Friday of the 8th week</td>
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<tr>
<td>8-week session</td>
<td>Friday of the 6th week</td>
</tr>
<tr>
<td>5-week session</td>
<td>Friday of the 4th week</td>
</tr>
</tbody>
</table>

The equivalent date (75% of the semester) will be used for sessions of other lengths. The specific last day to withdraw is published each semester in the Student Bulletin.

A student who officially withdraws will be awarded the grade of W provided the student’s attendance and academic performance are satisfactory at the time of official withdrawal. Students must file a withdrawal application with the College before they may be considered for withdrawal.

A student may not withdraw from a class for which the instructor has previously issued the student a grade of F or FN for nonattendance.

B. **Administrative Withdrawal:** An administrative withdrawal may be initiated when the student fails to meet College attendance requirements. The instructor will assign the appropriate grade on CTC Form 59 for submission to the registrar.

C. **Incomplete Grade:** The College catalog states, an incomplete grade may be given in those cases where the student has completed the majority of the course work but, because of personal illness, death in the immediate family, or military orders, the student is unable to complete the requirements for a course. Prior approval from the instructor is required before the grade of IP for Incomplete is recorded. A student who merely fails to show for the final examination will receive a zero for the final and an F for the course.

D. **Cellular Phones and Beepers:** Cellular phones and beepers will be turned off while the student is in the classroom or laboratory.

E. **Americans with Disabilities Act (ADA):** Disability Support Services provide services to students who have appropriate documentation of a disability. Students requiring accommodations for class are responsible for contacting the Office of Disability Support Services (DSS) located on the central campus. This service is available to all students, regardless of location. Explore the website at [www.ctcd.edu/disability-support](http://www.ctcd.edu/disability-support) for further information. Reasonable accommodations will be given in accordance with the federal and state laws through the DSS office.

F. **Instructor Discretion:** The instructor reserves the right of final decision in course requirements.

G. **Civility:** Individuals are expected to be cognizant of what a constructive educational experience is and respectful of those participating in a learning environment. Failure to do so can result in disciplinary action up to and including expulsion.
IX. COURSE OUTLINE

A. Unit One: Introductory Digital Concepts (Chapter One)
   1. Unit Objectives: Upon successful completion of this unit, the student will be able to:
      a. Explain the basic difference between digital and analog quantities.
      b. List the advantages and disadvantages of digital systems
      c. Show how voltage levels are used to represent digital quantities
      d. Describe serial and parallel data transmission and the benefits and shortcomings of each.

   2. Learning Activities:
      a. Read chapter 1. (F1)
      b. Classroom (Blackboard) lecture/discussion on Chapter 1 (C6)
      c. Post questions and responses to questions after reading assigned material. (C5)
      d. Answer the asterisked Problems at the end of chapter. Answers for these problems are in the back of the book. (F9)
      e. Take the chapter quiz at the Pearson (Prentice Hall) companion site. (F9)

B. Unit Two: Number Systems and Codes (Chapter Two)
   1. Unit Objectives: Upon successful completion of this unit, the student will be able to:
      a. Review the decimal number system.
      b. Count in the binary number system.
      c. Convert from decimal to binary and from binary to decimal.
      d. Apply arithmetic operations to binary numbers.
      e. Convert between the binary and hexadecimal number system.
      f. Convert between the binary and octal number systems.
      g. Express decimal numbers in binary coded decimal (BCD) form.
      h. Convert between the binary system and the Gray code.
      i. Interpret the American Standard Code for Information Interchange (ASCII).

   2. Learning Activities:
      a. Read chapter 2. (F1)
      b. Classroom (Blackboard) lecture/discussion on Chapter 2. (C6)
      c. Post questions and responses to questions after reading assigned material. (C5)
      d. View the PowerPoint slides for Chapter 2.
      e. Laboratory assignment: Student will complete the lab exercise(s) indicated. (C19, C20)
      f. Answer the asterisked Problems from 2-1 to 2-36 at the end of chapter.
Unit Three: Logic Gates (Chapter Three and Chapter 4)

1. **Unit Objectives:** Upon successful completion of this unit, the student will be able to:
   a. Describe the operation of the inverter, the AND gate and the OR gate.
   b. Describe the operation of the NAND gate and the NOR gate.
   c. Express the operation of NOT, AND, OR, NAND, and NOR gates using Boolean symbols.
   d. Describe the operation of the Exclusive-OR and Exclusive-NOR gates.
   e. Recognize and use both the distinctive shape logic gate symbols and the rectangular outline logic gate symbols of ANSI/IEEE Standard 91-1984.
   f. Construct timing diagrams showing the proper time relationships of inputs and outputs for the various logic gates.
   g. Make basic comparisons between the major IC technologies - CMOS and TTL.
   h. Explain how the various series within the CMOS and TTL families differ from one another.
   i. Define propagation delay time and fan-out.
   j. Use each logic gate in simple applications.
   k. Troubleshoot logic gates for proper inputs and outputs by using the logic probe.
   l. Describe the basic concepts of programmable logic.

2. **Learning Activities:**
   a. Read chapter 3, section 3-1 through 3-9 and Chapter 4, section 4-6. (F1)
   b. View the PowerPoint slides for Chapter 3.
   c. Classroom (Blackboard) lecture/discussion on Chapter 3 (C6)
   d. Laboratory assignment: Student will complete the lab exercise(s) indicated. (C19, C20)
   e. Answer the asterisked Problems, 3-1 through 3-19, at the end of Chapter 3. Answers for these problems are in the back of the book. (F9)
   f. Request and complete the Unit Quiz - Logic Gates for Chapter 3. (F4, F13)

Unit Four: Logic Boolean Algebra and Karnaugh Mapping (Chapter Three and Chapter 4)

1. **Unit Objectives:** Upon successful completion of this unit, the student will be able to:
   a. Apply the Single and Multivariable Theorems of Boolean algebra to circuits.
b. Apply Derived Expressions to logic circuits.
c. Apply DeMorgan’s theorems to Boolean expressions.
d. Evaluate Boolean expressions.
e. Simplify expressions by using the laws and rules of Boolean algebra.
f. Understand the difference between SOP and POS expressions and convert from one to the other.
g. Use a Karnaugh map to simplify Boolean expressions.
h. Utilize “don’t care” condition to simplify logic functions.
i. Apply Boolean algebra and the Karnaugh map method to a system application.

2. Learning Activities:
a. Read Chapter 3, sections 3-10 through 3-20, and Chapter 4, sections 4-1 through 4-9. (F1)
b. Review the PowerPoint slides for Chapter 3 and view the slides for Chapter 4.
c. Classroom (Blackboard) lecture/discussion on Chapter 3 (C6)
d. Laboratory assignment: Student will complete the lab exercise(s) indicated. (C19, C20)
e. Complete asterisked Problems 3-23 through 3-27, 3-33, 3-34, and 3-35. Answers for these questions, with the exception of 3-34, are found in the back of the textbook. Complete asterisked Problems 4-1 through 4-18. Answers for these problems are in the back of the book. (C9)
f. Take the Chapter Three quiz at the Pearson (Prentice Hall) companion site. (F9)
g. Request and complete the Unit Quiz – Boolean Simplification for Chapter 4. (F4, F13)

E. Unit Five: integrated Circuit Logic Families and Troubleshooting Integrated Circuits (Chapters Eight and Four)

1. Unit Objectives: Upon successful completion of this unit, the student will be able to:
   a. Understand IC terminology and read data sheets.
   b. Compare the characteristics of CMOS and TTL Logic Families.
   c. Determine fan-out for devices.
   d. Understand tri-state devices.
   e. Analyze basic combinational logic circuits to determine functionality
   f. Find faults in integrated circuits and external to the IC.
   g. Understand Parity generation and checking.

2. Learning Activities:
a. Read Chapter 8, sections 8-1 through 8-5. Read section 8-12. Read sections 8-16 through 8-19. (F1)
b. Read Chapter 4, sections 4-10 through 4-13 with emphasis on 4-13. (F1)
c. Review the PowerPoint slides for Chapter 8 and 4. (F1)
d. Ask/post any question on troubleshooting. (C6)
e. Work problems 8-1 through 8-21 at the end of Chapter 8. Do only the problems with an asterisk). Answers to asterisked questions are found in the back of the book).
f. Work Problems 4-39 through 4-49 at the end of Chapter 4. Do all of these problems. (C9)
g. Analyze a defective circuit (given to you by the instructor) and discuss your troubleshooting method to the class. (C5, C10)
h. Take the Chapter 4 quiz at the Pearson (Prentice Hall) companion site. (F9)

F. Unit Six: Latches and Flip-Flops
1. Unit Objectives: Upon successful completion of this unit, the student will be able to:
   a. Construct a 555 timer to operate as either an astable multivibrator or a one-shot.
   b. Construct a 555 to operate as a bistable device (clock).
   c. Use logic gates to construct basic latches.
   d. Explain the difference between an S-R latch and a D latch.
   e. Recognize the difference between a latch and a flip-flop.
   g. Understand edge-triggering and how it can be implemented.
   h. Understand the significance of propagation delays, set-up time, hold time, maximum operating frequency, minimum clock pulse widths, and power dissipation in the application of flip-flops.
   i. Analyze circuits for race conditions and the occurrence of glitches.
   j. Troubleshoot basic flip-flop circuits.
   k. Identify the basic forms of data movement in shift registers.
   l. Explain how serial in/serial out, serial in/parallel out, parallel in/serial out, and parallel in/parallel out shift registers operate.
   m. Describe how a bidirectional shift register operates.
   n. Determine the sequence of a Johnson counter.
   o. Construct a ring counter from a shift register.

2. Learning Activities:
   a. Read Chapter 5 of the textbook. (F1)
   b. View the PowerPoint slides for Chapter 5. (F1)
   c. Formulate and discuss/post any questions you have on Flip-Flops and timing circuits. (C5, F2)
   d. Complete the assigned labs. (C19, C20)
   e. Answer asterisked Problems 5-1 through 5-56 at the end of Chapter 5. Answers for these problems are in the back of the book. (C9)
   f. Take the Chapter 5 quiz at the Pearson (Prentice Hall) companion site. (F9)
   g. Request and complete the Unit Quiz – Flip-Flops and Latches for Chapter 5. (F4, F13)

G. Unit 7: Counters
1. Unit Objectives: Upon successful completion of this unit, the student will be able to:
   a. Describe the difference between an asynchronous and a synchronous
b. Analyze counter circuits.
c. Build an up/down counters (asynchronous and synchronous) to generate forward and reverse binary sequences.
d. Build a circuit to convert binary to decimal.
e. Use IC counters in various applications.
f. Use logic gates to decode any given state of a counter.
g. Design a counter that will have any specified sequence of states.
h. Use logic gates to decode any given state of a counter.
i. Determine the modulus of a counter and modify it.
j. Troubleshoot counters for various types of faults.
k. Interpret counter logic symbols that use dependency notation.

2. Learning Activities:
   a. Read Chapter 7 in the textbook. (F1)
   b. View the PowerPoint slides for Chapter 7. (F1)
   c. Formulate and discuss/post any questions you have on Counters. (C5, F2)
   d. Complete the assigned labs. (C19, C20)
   e. Answer the questions for flip-flops/latches in the lab manual. (C9)
   f. Do asterisked Problems 7-1 through 7-15 in the textbook at the end of Chapter 7. Answers for these problems are in the back of the book. (C9)
   g. Take the Chapter 7 quiz at the Pearson (Prentice Hall) companion site. (F9)
   h. Request and complete the Unit Quiz – Counters for Chapter 7. (F4, F13)

H. Unit 8: Arithmetic Circuits
   1. Unit Objectives: Upon successful completion of this unit, the student will be able to:
      a. Distinguish between half-adders and full-adders.
      b. Be able to represent signed numbers.
      c. Use 2’s complement in addition and subtraction.
      d. Use full-adders to implement multi-bit parallel binary adders.
      e. Build and troubleshoot an addition and subtraction circuits.
      f. Identify negative numbers generated by subtraction circuits.
      g. Understand hexadecimal arithmetic.
      h. Be aware of carry propagation in math circuits.

2. Learning Activities:
   a. Read Chapter 6 of the textbook. (F1)
   b. View the PowerPoint slides for Chapter 6. (F1)
   c. Formulate and discuss/post any questions you have on arithmetic circuits (C5, F2)
   d. Complete the assigned labs. (C19, C20)
   e. Answer the questions for adders and subtractors in the lab manual. (C9)
   f. Answer asterisked Problems 6-1 through 6-13. Answers for these problems are in the back of the book. (C9)
g. Complete the assigned labs. (C19, C20)
h. Take the Chapter 6 quiz at the Pearson (Prentice Hall) companion site. (F9)
i. Request and complete the Unit Quiz – Arithmetic Circuits for Chapter 6. (F4, F13)
Additional Notes & Requirements: RULES FOR ALL LABS

1. NO FOOD OR DRINK.
2. NO CANDY OR GUM.
3. NO HATS OR HEAD COVERS.
4. WORKSTATIONS WILL BE LEFT NEAT WITH THE CHAIR PUSHED IN, IN THE CORNER OF THE DESK.
5. NO WRITING ON THE DESKS.
6. IF YOU ARE VISITING WITH ANOTHER STUDENT, LEAVE THE LAB.
7. IF YOU ARE NOT IN THE LAB TO USE THE EQUIPMENT, LEAVE THE LAB.
8. IF YOU ARE NOT USING THE EQUIPMENT OR COMPUTERS ON THE DESKS, DO NOT PLAY WITH THEM.
9. ALL EQUIPMENT WILL BE RETURNED TO ITS PROPER PLACE (Even if you did not find it that way).
10. NO DISKS WILL BE BROUGHT IN THE LAB.
11. NO DISKS WILL LEAVE THE LAB. Return all NIDA disks to the proper location specified by the instructor.
12. ALL EQUIPMENT WILL BE TREATED WITH RESPECT. THERE WILL BE NO TOLERANCE FOR ABUSE TO THE EQUIPMENT.

VIOLATIONS OF ANY OF THESE SIMPLE RULES WILL RESULT IN EXPULSION FROM THE LAB AND/OR POINTS DEDUCTED FROM FINAL GRADE

a. Use logic gates to construct basic latches
b. Explain the difference between an S-R latch and a D latch
c. Recognize the difference between a latch and a flip-flop.
d. Explain how S-R, D, and J-K flip-flops differ.
e. Explain how edge-triggered and master-slave flip-flops differ.
f. Understand the significance of propagation delays, set-up time, hold time, maximum operating frequency, minimum clock pulse widths, and power dissipation in the application of flip-flops.
g. Apply flip-flops in basic applications.
h. Analyze circuits for race conditions and the occurrence of glitches.
i. Connect a 555 timer to operate as either an astable multivibrator or a one-
shot.

j. Connect a 555 to operate as a bistable device (clock)
k. Troubleshoot basic flip-flop circuits.
l. Apply one-shots in a system application.
m. Identify the basic forms of data movement in shift registers.
n. Explain how serial in/serial out, serial in/parallel out, parallel in/serial out, and parallel in/parallel out shift registers operate.
o. Describe how a bidirectional shift register operates.
p. Determine the sequence of a Johnson counter.
q. Set up a ring counter to produce a specified sequence.
r. Construct a ring counter from a shift register.

Use a shift register to implement a serial-to-parallel data converter.