I. INTRODUCTION

A. Introduction to a high level programming language. Includes structured programming and problem solving applicable to discrete electronic devices.

B. This course serves as a required or elective course on various degree plans. Curriculum plans for degrees and certificates are listed in the current Central Texas College catalog.

C. The delivery method of this course may be traditional lecture/lab, blended lecture/lab, or online.

D. Prerequisite: CETT 1325 Digital Fundamentals.

II. LEARNING OUTCOMES

Upon successful completion of this course, the student will be able to:

A. Design and simulate digital circuits using VHDL. (C1, C5, C6, C8, C19, C20, F1, F3, F8, F9, F12)

B. Load and test VHDL code for analysis. (C1, C5, C6, C8, C19, C20, F1, F3, F8, F9, F12).

C. Use structured programming methods to develop and execute high-level language programs which solve technical problems (C1, C5, C6, C8, C19, C20, F1, F3, F8, F9, F12).

III. INSTRUCTIONAL MATERIALS

A. The instructional materials identified for this course are viewable through www.cted.edu/books

B. Lecture Classes also require at least one USB storage device.
IV. COURSE REQUIREMENTS

A. Attend both lecture and lab or in the case of online delivery, be actively engaged in Blackboard and maintain constant progress.

B. Be prepared to participate in discussion, team projects/assignments and take unannounced assessments relating to the lecture materials.

C. Complete all exams/assessments.

D. Submit all assignments on time.

V. ASSESSMENTS

A. Student content mastery will be evaluated in the following areas:
   • Assessments (midterm exam, quizzes, projects, discussion etc.)
   • Final Assessment (final exam and/or semester project, participation)

B. Scheduled and unscheduled assessments will be given at the discretion of the instructor.

C. Exams/assessments may be composed of both subjective and objective questions plus computer output.

D. A student must take all exams/assessments. Both online and on campus students who know in advance that they will be absent due to school sponsored trips, military duty or orders, or any other valid reason, must arrange to take an early exam/assessment. Unexpected absences due to illness or other extenuating circumstances will require the student to contact the instructor about make-up work in lieu of the missed exam/assessment.

E. Students with unexcused absences will be given a zero for each missed assignment.

VI. SEMESTER GRADE COMPUTATIONS

<table>
<thead>
<tr>
<th>Course Requirements</th>
<th>Points</th>
<th>Points</th>
<th>Grade</th>
<th>Quality Points</th>
</tr>
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<tr>
<td>Assignments</td>
<td>300</td>
<td>900-1000</td>
<td>A-Superior</td>
<td>4</td>
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<tr>
<td>Assessments</td>
<td>300</td>
<td>800-899</td>
<td>B-Above Average</td>
<td>3</td>
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<tr>
<td>Final Assessment</td>
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<td>700-799</td>
<td>C-Average</td>
<td>2</td>
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<tr>
<td></td>
<td>600 - 699</td>
<td>D-Passing, but unsatisfactory</td>
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<tr>
<td>TOTAL</td>
<td>1000</td>
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<tr>
<td>0 - 599</td>
<td>F-Failure</td>
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VII. NOTES AND ADDITIONAL INSTRUCTIONS FROM THE INSTRUCTOR

A. **Information on the following Academic Policies, as described in the CTC Course Catalog will be followed:**
   1. Withdrawals
   2. Grading
   3. Class Attendance and Course Progress
   4. Scholastic Honesty

B. **Cell Phones and Pagers:** Students will silence cell phones and mobile devices while in the classroom or lab.

C. **Americans with Disabilities Act (ADA):** Disability Support Services provide services to students who have appropriate documentation of a disability. Students requiring accommodations for class are responsible for contacting the Office of Disability Support Services (DSS) located on the central campus. This service is available to all students, regardless of location. Review the website at [www.ctcd.edu/disability-support](http://www.ctcd.edu/disability-support) for further information. Reasonable accommodations will be given in accordance with the federal and state laws through the DSS office.

D. **Instructor Discretion:** The instructor reserves the right of final decision in course requirements and may make changes to the course outline and/or assignments as needed.

E. **Civility:** Individuals are expected to be aware of what a constructive educational experience is and be respectful of those participating in a learning environment. Failure to do so can result in disciplinary action up to and including expulsion.
VIII. COURSE OUTLINE

A. Lesson One: What is VHDL

1. Learning Outcomes: Upon successful completion of this unit the student will be able to:
   a. Describe the history of VHDL
   b. Identify the various VHDL version
   c. Describe VHDL design flow.
   d. Discuss the various EDA tools available and how code is translated into a circuit.
   e. Identify the elements of VHDL syntax
   f. Analyze number and character representation in VHDL.

2. Learning Activities:
   a. Research and discuss the topics of the lesson in class and in an online collaborative discussion forum (C7, C8, C9, C15, C18, F1, F9, F10, F13)
   b. Perform skills and functions in the section (C1, C5, C7, C8, C9, C16, C18, F1, F9, F10, F13)

3. Unit Outline: Follow the sequence of unit objectives.

B. Lesson Two: Code Structure

1. Learning Outcomes: Upon successful completion of this unit the student will be able to:
   a. Identify the basic VHDL units.
   b. Identify VHDL libraries and packages.
   c. Describe the Entity and Architecture elements
   d. Analyze VHDL examples.
   e. State the new features in VHDL 2008.

2. Learning Activities:
   a. Research and discuss the topics of the Lesson in class and in an online collaborative discussion forum (C7, C8, C9, C15, C18, F1, F9, F10, F13)
   b. Perform skills and functions in the section (C1, C5, C7, C8, C9, C16, C18, F1, F9, F10, F13)

3. Unit Outline: Follow the sequence of the unit objectives.
C. **Lesson Three:** Data Types

1. **Learning Outcomes:** Upon successful completion of this unit the student will be able to:
   a. Define VHDL objects.
   b. Explain the use of Data Types and Packages.
   c. Create user defined Scalar and Array types.
   d. Describe the steps and activities involved in the enumeration process.
   e. Demonstrate the difference between legal and illegal assignments.
   f. Discuss the difference between integer and enumerated indexing.

2. **Learning Activities:**
   a. Research and discuss the topics of the Lesson in class and in an online collaborative discussion forum (C7, C8, C9, C15, C18, F1, F9, F10, F13)
   b. Perform skills and functions in the section (C1, C5, C7, C8, C9, C16, C18, F1, F9, F10, F13)

3. **Unit Outline:** Follow the sequence of the unit objectives

D. **Lesson Four:** Programming for Security Professionals

1. **Learning Outcomes:** Upon successful completion of this unit the student will be able to:
   a. Discuss the logical and arithmetic operators used in digital systems.
   b. Identify the Predefined attributes in VHDL.
   c. Implement user defined attributes.
   d. Contrast group attributes with individual attributes

2. **Learning Activities:**
   a. Research and discuss the topics of the Lesson in class and in an online collaborative discussion forum (C7, C8, C9, C15, C18, F1, F9, F10, F13)
   b. Perform skills and functions in the section (C1, C5, C7, C8, C9, C16, C18, F1, F9, F10, F13)

3. **Unit Outline:** Follow the sequence of the unit objectives

E. **Lesson Five:** Concurrent Code in VHDL

1. **Learning Outcomes:** Upon successful completion of this unit the student will be able to:
   a. Identify concurrent coeds in VHDL constructs
   b. Discuss When, Select, and Generate commands.
   c. Implement arithmetic circuits.
   d. Investigate multiple signal assignments in a VHDL code.
e. Create circuits using multiple signal assignments.

2. Learning Activities:
   a. Research and discuss the topics of the Lesson in class and in an online collaborative discussion forum (C7, C8, C9, C15, C18, F1, F9, F10, F13)
   b. Perform skills and functions in the section (C1, C5, C7, C8, C9, C16, C18, F1, F9, F10, F13)

3. Outline: Follow the sequence of the unit objectives

F. Lesson Six: Sequential Coding

1. Learning Outcomes: Upon successful completion of this unit the student will be able to:
   a. Identify sequential codes in VHDL constructs
   b. Employ If, Wait, Loop, and Case, statements in VHDL.
   c. Explain the difference between Case and Select.
   d. Implement circuits with sequential code.

2. Learning Activities:
   a. Research and discuss the topics of the Lesson in class and in an online collaborative discussion forum (C7, C8, C9, C15, C18, F1, F9, F10, F13)
   b. Perform skills and functions in the section (C1, C5, C7, C8, C9, C16, C18, F1, F9, F10, F13)

3. Outline: Follow the sequence of the unit objectives

G. Lesson Seven: Signals and Variables

1. Learning Outcomes: Upon successful completion of this unit the student will be able to:
   a. Explain the difference between Signals and Variables.
   b. Investigate methods to minimize the number of constructs in VHDL.
   c. Create code employing dual edge circuits.
   d. Describe multiple signal assignments.
   e. Analyze code or combinational and sequential elements.

2. Learning Activities:
   a. Research and discuss the topics of the Lesson in class and in an online collaborative discussion forum (C7, C8, C9, C15, C18, F1, F9, F10, F13)
   b. Perform skills and functions in the section (C1, C5, C7, C8, C9, C16, C18, F1, F9, F10, F13)

3. Unit Outline: Follow the sequence of the unit objectives
H. Lesson Eight: Packages and Components

1. Learning Outcomes: Upon successful completion of this unit the student will be able to:
   a. State the difference between Packages and Components.
   b. Explain how packages and components can be used in System Level VHDL
   c. Identify and employ Generic Code in programs.
   d. Describe the use of configuration in hierarchic designs.
   e. Use the Block statement in code.
   f. Recognize application of the Function command.

2. Learning Activities:
   a. Research and discuss the topics of the Lesson in class and in an online collaborative discussion forum (C7, C8, C9, C15, C18, F1, F9, F10, F13)
   b. Perform skills and functions in the section (C1, C5, C7, C8, C9, C16, C18, F1, F9, F10, F13)

3. Outline: Follow the sequence of the unit objectives